

What Is Claimed Is:

1. An array substrate for a liquid crystal display device, comprising:

a substrate;

a plurality of thin film transistors formed on the substrate, each thin film transistor comprises a gate electrode, a source electrode and a drain electrode;

a plurality of gate lines arranged in one direction on the substrate, each gate line connected with the gate electrodes of the plurality of thin film transistors and each gate line has a gate pad disposed at a first end thereof;

a plurality of data lines arranged perpendicular to the plurality of gate lines on the substrate, each data line connected to the source electrodes of the plurality of thin film transistors and each data line has a data pad disposed at a first end thereof;

a plurality of pixel electrodes located at pixel regions defined by intersections of the plurality of gate lines and the plurality of data lines, each pixel electrode contacting each drain electrode of the plurality of thin film transistors;

a first data shorting bar arranged parallel with the plurality of gate lines at the first end of the data lines;

a second data shorting bar arranged parallel with the plurality of gate lines at the first end of the gate lines and spaced apart from the first data shorting bar;

a plurality of first connectors electrically connecting the odd numbered data lines to the first data-shortening bar;

a plurality of second connectors electrically connecting the even numbered data lines to the second data shortening bar; and

a plurality of patterned insulating segments formed over the first shortening bar and below the plurality of second connectors, wherein each patterned insulating segment is disposed at an intersection between the first data shortening bar and each second connector.

2. The array substrate according to Claim 1, wherein each patterned insulating segment includes at least a passivation layer, a metal layer, an ohmic contact layer, and an active layer.

3. The array substrate according to Claim 1, wherein a side portion of each drain electrode of the plurality of thin film transistors is exposed to contact each pixel electrode.

4. The array substrate according to Claim 1, wherein the first connectors, the second connectors, and the pixel electrodes are formed of at least one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

5. The array substrate according to Claim 1, wherein the data lines and the data pads include at least a molybdenum (Mo) material.

6. The array substrate according to Claim 1, wherein each of the first connectors and each of the second connectors contact the data pads through data pad contact holes.

7. A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate;

patterning the first metal layer to form a gate line, a gate electrode, a gate pad, a first shorting bar, and a second shorting bar;

forming a gate insulation layer, a pure amorphous silicon layer, a doped amorphous silicon layer and a second metal layer to cover the patterned first metal layer;

patterning the second metal layer and the doped amorphous silicon layer to form first, second and third through-holes and first and second grooves to expose a portion of the pure amorphous silicon layer, the first and second grooves creating an isolated portions of the second metal layer;

forming a passivation layer to cover the patterned second metal layer;

forming a source electrode, a drain electrode, a data line, a data pad, an insulating segment, and first, second and third contact holes; and

forming a pixel electrode, a first connector and a second connector of a transparent conductive material.

8. The method of fabricating an array substrate according to Claim 7, wherein the gate electrode extends from the gate line, the gate pad is arranged at a first end of the gate line, and the first shorting bar and the second shorting bar are spaced apart from each other and arranged parallel with the gate line.

9. The method of fabricating an array substrate according to Claim 7, wherein the source electrode extends from the data line, and the drain electrode is spaced apart from the source electrode.

10. The method of fabricating an array substrate according to Claim 7, wherein the data pad is arranged at a first end of the data line, and the insulating segment is formed over the first shorting bar.

11. The method of fabricating an array substrate according to Claim 7, wherein the first contact hole penetrates the data pad, the second contact hole exposes a

portion of the first shorting bar, and the third contact hole exposes a portion of the second shorting bar.

12. The method of fabricating an array substrate according to Claim 7, wherein the pixel electrode is connected with the drain electrode and is located in a pixel region defined by the gate line and the data line.

13. The method of fabricating an array substrate according to Claim 7, wherein the first connector electrically connects an odd numbered data line to the first shorting bar, and the second connector electrically connects an even numbered data lines to the second shorting bar.

14. The method of fabricating an array substrate according to Claim 7, wherein the first connector and the second connector contact the data pad through the first contact hole.

15. The method of fabricating an array substrate according to Claim 14, wherein the first connector contacts the first shorting bar through the second contact hole.

16. The method of fabricating an array substrate according to Claim 14, wherein the second connector contacts the second shorting bar through the third contact hole.

17. The method of fabricating an array substrate according to Claim 7, wherein the insulating segment is formed at a crossover point of the first shorting bar and the second connector.

18. The method of fabricating an array substrate according to Claim 17, wherein the insulating segment is disposed between the first shorting bar and the second connector.

19. The method of fabricating an array substrate according to Claim 18, wherein the insulating segment includes patterned layers comprising the passivation layer, the second metal layer, the doped amorphous silicon layer and the pure amorphous silicon layer.

20. The method of fabricating an array substrate according to Claim 7, wherein the transparent conductive material includes at least one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

21. The method of fabricating an array substrate according to Claim 7, wherein the first hole is formed over the gate electrode.

22. The method of fabricating an array substrate according to Claim 7, wherein the second hole is formed over the first shorting bar.

23. The method of fabricating an array substrate according to Claim 7, wherein the third hole is formed over the second shorting bar.

24. The method of fabricating an array substrate according to Claim 7, wherein the isolated metal layer is formed over the first shorting bar.

25. The method of fabricating an array substrate according to Claim 24, wherein the first groove and the second groove are formed on opposite sides of the isolated metal layer.

26. The method of fabricating an array substrate according to Claim 24, wherein the first groove is formed in a portion of the second metal layer between the first shorting bar and the second shorting bar.

27. The method of fabricating an array substrate according to Claim 7, wherein the second metal layer includes at least molybdenum (Mo) material.

28. An array substrate having thin film transistors, pixel electrodes, gate lines and data lines, wherein each thin film transistor is formed at a crossover point of each pairs of gate lines and data lines, and wherein each pixel electrode is formed in a pixel region defined by each of the pairs of gate lines and data lines, the array substrate comprising:

- a plurality of data pads formed at a first end of the data lines and connected thereto, the data pads including odd numbered data pads and even numbered data pads, each data pad having a first contact hole;

- a first shorting bar formed adjacent to the data pads and arranged perpendicular to the data lines;

- a second shorting bar spaced apart from and arranged parallel with the first shorting bar;

- a gate insulation layer covering the gate lines, the first shorting bar, and the second shorting bar, the gate insulation layer having second and third contact holes, wherein the second contact holes are formed over the first shorting bar, and wherein the third contact holes are formed over the second shorting bar;

- a first connector connecting the odd numbered data pads to the first shorting bar through the first contact hole and second contact hole;

a plurality of second connectors each crossing the first shorting bar and connecting the even numbered data pads to the second shorting bar through the first contact hole and the third contact hole; and

a plurality of island-shaped insulating segments formed between the first shorting bar and each second connector at each intersection of the first shorting bar and the second connector, each island-shaped insulating segment electrically insulating the first shorting bar from each second connector.

29. The array substrate according to Claim 28, wherein the pixel electrodes, the first connector, and the second connectors are formed of one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

30. The array substrate according to Claim 29, wherein each island-shaped insulating segment includes the passivation layer, the second metal layer, the doped amorphous silicon layer, and the pure amorphous silicon layer.

31. A liquid crystal display device, comprising:

a substrate;

a plurality of gate lines on the substrate;

a plurality of data lines on the substrate and disposed perpendicular to the

plurality of gate lines;

a first data shorting bar arranged parallel with the plurality of gate lines at a first end of the data lines;

a second data shorting bar arranged parallel with the plurality of gate lines at a first end of the gate lines and spaced apart from the first data shorting bar;

a plurality of first connectors electrically connecting odd numbered data lines to the first data-shortening bar;

a plurality of second connectors electrically connecting even numbered data lines to the second data shorting bar; and

a plurality of patterned insulating segments formed over the first shorting bar and below the plurality of second connectors, wherein each patterned insulating segment is disposed at an intersection between the first data shorting bar and each second connector.

32. The liquid crystal display device according to Claim 31, wherein each patterned insulating segment includes a passivation layer, a second metal layer, a doped amorphous silicon layer, and a pure amorphous silicon layer.